Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory cell with at least two detectable states among which is an unprogrammed state, comprising:

a first branch in series between first and second terminals of application of a read voltage, the first branch including:

a pre-read stage comprising, in parallel, two switchable resistors having different values with a predetermined first difference; and

a programming stage that includes a ~~polysilicon~~ first ~~programming resistor~~programmable resistive element having a terminal accessible by a first programming circuit capable of causing an irreversible decrease in a resistance value of the first ~~programming resistor~~programmable resistive element.

2. (Original) The memory cell of claim 1, wherein said decrease in the programming resistance value is predetermined and chosen to be greater than said first difference between the resistances of the pre-read stage.

3. (Currently Amended) The memory cell of claim 1, wherein the first programming circuit includes switches capable of applying a programming voltage greater than the read voltage across the first ~~programming resistor~~programmable resistive element.

4. (Original) The memory cell of claim 1, comprising at least one switch for isolating the pre-read stage with respect to the programming stage.

5. (Original) The memory cell of claim 1, wherein a reading of the cell state is performed in two successive steps during which said switchable resistors of the pre-read stage are alternately selected.

6. (Currently Amended) The memory cell of claim 5, wherein said terminal of the first ~~programming resistor~~programmable resistive element forms a read terminal of the cell capable of being connected to a first terminal of a read amplifier having a second terminal receiving at least one reference voltage chosen to be an intermediary level between the voltage level taken by the read terminal in the two read phases, while the first ~~programming resistor~~programmable resistive element is in an unprogrammed state.

7. (Currently Amended) The memory cell of claim 1, wherein the first branch includes a first transistor, the memory cell further comprising a second branch that includes a pre-read stage comprising, in parallel, two switchable resistors having different values with a predetermined first difference; a programming stage that includes a ~~polysilicon~~ second ~~programming resistor~~programmable resistive element having a terminal accessible by a second programming circuit capable of causing the irreversible decrease in a resistance value of the second programmable resistive element~~resistor~~; and a second transistor assembled as a flip-flop with the first transistor, the first ~~programming resistor~~programmable resistive element being connected to the second terminal by the second transistor and the second ~~programming resistor~~programmable resistive element being connected to the second terminal by the first transistor.

8. (Original) The memory cell of claim 7, wherein the switchable resistors of the second branch are controllable at the same time as the switchable resistors of the first branch, so that the respective values of the resistors selected in each of the branches are inverted.

9. (Currently Amended) The memory cell of claim 7, wherein the irreversible decrease to be applied to the ~~programming resistors~~programmable resistive elements

is chosen to be greater than the sum of the difference between the pre-read resistances and of a third nominal value difference between the ~~programming resistors~~programmable resistive elements in an unprogrammed state.

10. (Currently Amended) A method for reading a memory cell with at least two detectable states among which is an unprogrammed state, the memory cell including a first branch in series between first and second terminals of application of a read voltage, the first branch including: a pre-read stage comprising, in parallel, two switchable resistors having different values with a predetermined first difference; and a programming stage that includes a ~~polysilicon~~ first ~~programming resistor~~programmable resistive element having a terminal accessible by a first programming circuit capable of causing an irreversible decrease in a resistance value of the first ~~programming resistor~~programmable resistive element, the method comprising performing two successive read steps during which said switchable resistors of the pre-read stage are respectively selected.

11. –23. (Canceled)

24. (Currently Amended) The method of claim 10 wherein:

the first read step includes driving the first ~~programming resistor~~programmable resistive element with a first current from a first one of the switchable resistors and measuring a first electrical quantity at the first ~~programming resistor~~programmable resistive element;

the second read step includes driving the first ~~programming resistor~~programmable resistive element with a second current from a second one of the switchable resistors and measuring a second electrical quantity at the first ~~programming resistor~~programmable resistive element, the method further comprising:

detecting whether a memory state of the memory cell is a first memory state or a second memory state by comparing the first electrical quantity with the second electrical quantity.

25. (Previously Presented) The method of claim 24 wherein the detecting step includes:

detecting the first memory state by detecting that the first electrical quantity logically equals the second electrical quantity; and

detecting the second memory state by detecting that the first electrical quantity does not logically equal the second electrical quantity.

26. (Previously Presented) The method of claim 25 wherein detecting the first memory state includes detecting that the first and second electrical quantities are logical high values, the method further comprising detecting a third memory state by detecting that the first and second electrical quantities are logical low values.

27. (Previously Presented) The method of claim 24 wherein the detecting step includes:

detecting the first memory state by detecting that the first electrical quantity is greater than the second electrical quantity; and

detecting the second memory state by detecting that the first electrical quantity is less than the second electrical quantity.

28. (Currently Amended) The method of claim 10, wherein the memory cell further includes a second branch that includes a pre-read stage including, in parallel, two switchable resistors having different values with the first difference; and a programming stage that includes a second ~~programming resistor~~programmable resistive element having a terminal accessible by a second programming circuit capable of causing an irreversible decrease in a resistance value of the second programmable resistor, the method further comprising performing two successive read steps during which the switchable resistors of the pre-read stage of the second branch are respectively selected.

29. (Previously Presented) The method of claim 28, wherein the switchable resistors of the second branch are controllable at the same time as the switchable resistors of the first branch, so that the respective values of the resistors selected in each of the branches are inverted.

30. (Currently Amended) A memory device, comprising:

a memory cell with at least two detectable states among which is an unprogrammed state, the memory cell including:

a first branch in series between first and second terminals of application of a read voltage, the first branch including:

a pre-read stage including, in parallel, two switchable resistors having different values with a first difference; and

a programming stage that includes a first ~~programming resistor~~programmable resistive element having a terminal accessible by a first programming circuit structured to cause ~~an irreversible decrease~~a change in a resistance value of the first ~~programming resistor~~programmable resistive element.

31. (Currently Amended) The memory device of claim 30, wherein said ~~decrease~~ change in the programming resistance value is predetermined and chosen to be greater than said first difference between the resistances of the pre-read stage.

32. (Currently Amended) The memory device of claim 30, wherein the first programming circuit includes switches capable of applying a programming voltage greater than the read voltage across the first ~~programming resistor~~programmable resistive element.

33. (Previously Presented) The memory device of claim 30, comprising a switch for isolating the pre-read stage with respect to the programming stage.

34. (Previously Presented) The memory device of claim 30, wherein a reading of the cell state is performed in two successive steps during which said switchable resistors of the pre-read stage are alternately selected.

35. (Currently Amended) The memory device of claim 34, wherein said terminal of the first ~~programming resistor~~programmable resistive element forms a read terminal of the cell and is connected to a first terminal of a read amplifier having a second terminal receiving at least one reference voltage chosen to be an intermediary level between the voltage level taken by the read terminal in the two read phases, while the first ~~programming resistor~~programmable resistive element is in an unprogrammed state.

36. (Currently Amended) The memory device of claim 30, wherein the first branch includes a first transistor, the memory cell further comprising a second branch that includes a pre-read stage comprising, in parallel, two switchable resistors having different values with a predetermined first difference; a programming stage that includes a ~~polysilicon~~ second ~~programming resistor~~programmable resistive element having a terminal accessible by a second programming circuit capable of causing ~~the irreversible decrease~~a change in a resistance value of the second programmable resistor; and a second transistor assembled as a flip-flop with the first transistor, the first ~~programming resistor~~programmable resistive element being connected to the second terminal by the second transistor and the second ~~programming resistor~~programmable resistive element being connected to the second terminal by the first transistor.

37. (Previously Presented) The memory device of claim 36, wherein the first branch includes first and second switches coupled respectively to first and second resistors of the switchable resistors of the first branch and the second branch includes third and fourth switches coupled respectively to third and fourth resistors of the switchable resistors of the second branch, wherein the first and fourth resistors have substantially identical resistance values, the second and third resistors have substantially identical resistance values, the first and third switches have respective control terminals coupled to one another and controlled by a first control signal, and

the second and fourth switches have respective control terminals coupled to one another and controlled by a second control signal.

38. (Currently Amended) The memory device of claim 36, wherein the ~~irreversible decrease to be applied to~~change in the resistance values of the ~~programming resistors~~programmable resistive elements is chosen to be greater than the sum of the difference between the pre-read resistances and of a third nominal value difference between the ~~programming resistors~~programmable resistive elements in an unprogrammed state.

39. (New) The memory device of claim 30 wherein the first programmable resistive element is a polysilicon resistor.

40. (New) The memory device of claim 30 wherein the first programmable resistive element is one-time programmable.

41. (New) The memory device of claim 30 wherein the first programming circuit is structured to cause an irreversible decrease in the resistance value of the first programmable resistive element.

42. (New) The memory cell of claim 1 wherein the first programmable resistive element is a polysilicon resistor.

43. (New) A memory device, comprising:

a memory cell with at least two detectable states among which is an unprogrammed state, the memory cell including:

a first pre-read stage including, in parallel, first and second switchable resistors having different values with a first difference;

a first programmable resistive element coupled to the pre-read stage and having a first terminal; and

a first programming circuit structured to program the first programmable resistance element by providing to the first terminal a programming voltage sufficient to cause a change in a resistance value of the first programmable resistive element.

44. (New) The memory device of claim 43, wherein said change in the programming resistance value is predetermined and chosen to be greater than said first difference between the resistances of the pre-read stage.

45. (New) The memory device of claim 43, wherein the first programming circuit includes a switch connected between a programming terminal and the first terminal of the first programmable resistance element, the programming voltage being greater than a read voltage applied by the first pre-read stage across the first programmable resistive element.

46. (New) The memory device of claim 43, further comprising a switch positioned between the first pre-read stage and the first terminal of the first programmable resistance element, the switch being structured to isolate the pre-read stage from the programming voltage.

47. (New) The memory device of claim 43, wherein the first pre-read stage includes a first switch in series with a first one of the switchable resistors and a second switch in series with a second one of the switchable resistors, the first and second switches being controlled respectively by first and second pre-read signals that cause a reading of the cell state to be performed in two successive phases during which said first and second switches of the pre-read stage are alternately selected.

48. (New) The memory device of claim 47, wherein said first terminal of the first programmable resistive element forms a read terminal of the cell, the memory device further comprising a read amplifier having a first terminal connected to the first terminal of the first programmable resistive element, and a second terminal receiving a reference voltage chosen to

be an intermediary level between voltage levels taken by the read terminal in the two read phases, while the first programmable resistive element is in an unprogrammed state.

49. (New) The memory device of claim 43, further comprising:

a first transistor coupled between a second terminal of the first programmable resistance element and a voltage reference;

a second pre-read stage comprising, in parallel, third and fourth switchable resistors having different values with the first difference;

a second programmable resistive element coupled to the second pre-read stage and having first and second terminals;

a second programming circuit structured to provide to the first terminal of the second programmable resistive element a programming voltage sufficient to cause a change in a resistance value of the second programmable resistive element; and

a second transistor assembled as a flip-flop with the first transistor and coupled between the second terminal of the second programmable resistance element and the voltage reference.

50. (New) The memory device of claim 49, wherein the first pre-read stage includes first and second switches coupled respectively to the first and second switchable resistors and the second pre-read stage includes third and fourth switches coupled respectively to the third and fourth switchable resistors, wherein the first and fourth switchable resistors have substantially identical resistance values, the second and third switchable resistors have substantially identical resistance values, the first and third switches have respective control terminals coupled to one another and controlled by a first control signal, and the second and fourth switches have respective control terminals coupled to one another and controlled by a second control signal.

51. (New) The memory device of claim 49, wherein the change in the resistance values of the programmable resistive elements is chosen to be greater than the sum of

the difference between the pre-read resistance values and of a third nominal value difference between the programmable resistive elements in an unprogrammed state.

52. (New) The memory device of claim 43 wherein the first programmable resistive element is a polysilicon resistor.

53. (New) The memory device of claim 43 wherein the first programmable resistive element is one-time programmable.

54. (New) The memory device of claim 43 wherein the first programming circuit is structured to cause an irreversible decrease in the resistance value of the first programmable resistive element.